Institution: Liverpool John Moores University

Unit of Assessment: 13 Electrical and Electronic Engineering, Metallurgy and Materials

Title of case study: Impact of research into pulse techniques on new generation of Flash memory devices

1. Short summary of the case study

Using high-k dielectric enables the Flash memory industry to develop sub-28-nm products, but the high density of defects in high-k dielectric is a major challenge for product qualification, since the existing characterisation techniques are not suitable. The new pulse techniques, developed by the Microelectronics Research Group (RG1), overcome this challenge and have been extensively used by the Memory Devices Consortium (including Intel, Micron and Samsung) at IMEC (the Inter-University Microelectronics Research Centre in Leuven, Belgium) for the development of new Flash memory products in this REF period. This benefits the global Flash memory industry by providing guidance for material selection, process screening, device structure optimisation, and qualification procedure improvement.

2. Underpinning research

Flash memory industry has generated over $ 20-bilillon in revenue in 2012. Using high-k dielectric is essential for achieving a sub-28-nm feature size. However, the large defect density in the high-κ materials causes complex electron trapping/detrapping and is limiting its application. Novel techniques are needed to characterise these defects for the qualification and screening of new materials, processes, and device structures when developing the next generation memory devices.

The existing techniques for characterising electron trapping in high-k materials were developed for the logic CMOS devices, which targeted the thin high-k gate dielectric stack in contact with the substrate directly. These techniques are of limited use for memory devices, which use much thicker high-k layers and have more complicated gate dielectric structures: the slow DC techniques cannot probe the fast trapping/detrapping; the existing pulse techniques cannot probe the deep traps in the dielectric bulk. These techniques are not suitable for characterising the interaction of traps in different layers either, and such interaction has a direct impact on the memory performance. Since 2007, Dr W. Zhang (Reader at the University) has led the research in proposing and demonstrating new pulse techniques that overcome these shortcomings, as detailed below.

Limitation of charging/discharge time: In order to charge/discharge the electron traps deep into high-k materials, a time longer than 1000 sec is typically needed. On the other hand, to avoid disturbing the shallow traps during the measurement itself, a measurement must be completed within microseconds. None of the existing techniques can meet these conflicting time requirements simultaneously [R1.1-R1.6].

The RG1 made a breakthrough by developing a new 2-pulse technique, which demonstrated, for the first time ever, that electron traps can be fully charged/discharged throughout the dielectric stack by applying a suitable bias between the two pulses, and the measurements, taken on the fast pulse edges, can “freeze” the trapping/detrapping [R1.1]. This new technique can successfully extract the energy regions and spatial locations of electron traps over the whole high-k dielectric stacks used in new generations of Flash memory, which is also confirmed by detailed modelling and simulation [R1.2].

Lack of defect energy profiles: Detailed energy profile of electron traps in high-k materials is required for characterising the memory performance and, in turn, the qualification of new materials, processes, and device structures. Existing techniques can only either probe a limited energy range above silicon conduction band edge, or are limited to traps near the substrate interface [R1.3].

Based on the success of the 2-pulse technique, a multi-pulse technique was further developed specifically for probing the detailed energy distribution of traps. Traps were first fully

charged and then discharged, level by level, under multiple consecutively decreasing biases. For the first time ever, the energy distribution across the dielectric band gap is successfully obtained [R1.3].

These pulse techniques have since been used in the development of new memory devices in a number of aspects, including Material selection, Process screening, Device structure optimisation, and Qualification procedure (e.g. [R1.1-R1.6]).

The research above was carried out in collaboration with the Memory Devices Consortium at IMEC, whose main roles are identifying the inadequacy of existing techniques, providing in-kind support including test samples, and demonstrating the capability of the pulse techniques to users. In addition, IMEC served as a platform for delivering the impact, as detailed in section 4.

3. References to the research

('**' denotes the three papers that best illustrate the quality of the underpinning research)

[R1.1] **X. F. Zheng, W. D. Zhang, B. Govoreanu, D. Ruiz Aguado, J. F. Zhang, J. van Houdt, "Energy and spatial distributions of electron traps throughout SiO2/Al2O3 stacks as the IPD in Flash memory application," *IEEE Transactions on Electron Devices*, vol. 57, pp. 288-296, 2010 (d.o.i.:10.1109/TED.2009.2035193).

[R1.2] D. Ruiz Aguado, B. Govoreanu, W. D. Zhang, M. Jurczak, K. De Meyer, J. van Houdt, "A novel trapping/detrapping model for defect profiling in high-k materials using the two-pulse capacitance-voltage technique," *IEEE Transactions on Electron Devices*, vol. 57, pp. 2726-2735, 2010 (d.o.i.: 10.1109/TED.2010.2063292).

[R1.3] **X. F. Zheng, W. D. Zhang, B. Govoreanu, J. F. Zhang, J. van Houdt, "A new multi-pulse technique for probing electron trap energy distribution in high-κ materials for Flash memory application," *IEEE Transactions on Electron Devices*, vol. 57, pp. 2484-2492, 2010 (d.o.i.:10.1109/TED.2010.2062520).

[R1.4] X. F. Zheng, C. Robinson, W. D. Zhang, J. F. Zhang, B. Govoreanu, J. van Houdt, "Electron trapping in HfAlO high-*κ* stack for Flash memory applications: an origin of V_{th} window closure during cycling operations," *IEEE Transactions on Electron Devices*, vol. 58, pp. 1344-1351, 2011 (d.o.i.: 10.1109/TED.2011.2115244).

[R1.5] **B. J. Tang, C. Robinson, W. D. Zhang, J. F. Zhang, R. Degraeve, P. Blomme, M. Toledano-Luque, G. Van den Bosch, B. Govoreanu, J. Van Houdt, "Read and pass disturbance in the programmed states of floating gate flash memory cells with high-κ interpoly gate dielectric stacks", *IEEE Transactions on Electron Devices*, vol. 60, pp. 2261-2267, 2013 (d.o.i.: 10.1109/TED.2013.2264163).

[R1.6] B. J. Tang, W. D. Zhang, J. F. Zhang, G. van den Bosch, M. Toledano-Luque, B. Govoreanu, J. van Houdt, "Investigation of abnormal VTH/VFB shifts under operating conditions in Flash memory cells with Al2O3 high-κ gate stacks," *IEEE Transactions on Electron Devices*, vol. 59, pp. 1870-1877, 2012 (d.o.i.: 10.1109/TED.2012.2194294).

4. Details of the impact

This case study shows how the RG1's work contributes to new technology/product development by directly engaging with the Memory Devices Consortium through secondments of the University researchers to IMEC. The members of this Consortium include Intel, Micron, Samsung, SanDisk, SK Hynix, and Toshiba.

Between 2009 and 2012, the University and IMEC have signed three official collaboration agreements to work on the new generation of memory devices [C1.1-C1.3], involving the following:

- IMEC provided in-kind support for the work at the University. The test samples supplied to RG1 were costed by IMEC at 900,000 Euros, as specified under the heading of 'Article

3 FEES' in the three agreements [C1.1-C1.3]. In return, RG1 researchers spent six-months per person per annum at IMEC to work together with the industrial partners. RG1 researchers, W.Zhang and B.Tang, worked for cumulative two person-years at IMEC.

- The research plans were defined and tailored specifically to meet the most important needs of the industrial partners: implement and qualify the high-k dielectric for Flash memory. Discussions between researchers from the University, IMEC, and industrial partners were carried out through the regular progress meetings.
- Test samples were manufactured at IMEC to the highest standard according to the industrial partners' requirements in order to investigate issues of their major concern during new technology and product development. These state-of-the-art samples were supplied to the University, so that its work is of direct relevance to the Consortium.

Utilization of the development work at IMEC has led to the successful introduction of high-k dielectrics for new generations of commercial flash memory technology. For example, Intel/Micron has used the high-k dielectrics in their 20-nm production since 2011, "which has been a major breakthrough for the Flash memory industry" [C1.4].

The specific contributions of the RG1 research to the development work are:

- Proposing and demonstrating the pulse techniques for probing the defects in memory-relevant high-k dielectrics and using them in qualifying memory devices [C1.4, C1.5];
- Disseminating these techniques and results to the Consortium members through progress reports, oral and poster presentations at industrial review meetings, and seminars. For example, W.Zhang was invited to give a seminar on the 2-pulse technique not only to the industrial assignees at IMEC, but also to engineers at Intel's base in California, USA [C1.6].
- Implementing these techniques at IMEC [C1.6].

As confirmed by Dr Van Houdt, IMEC Flash Memory Director, in [C1.4], "These pulse techniques were extensively used in the qualification of new Flash memory technology and were proven as powerful and essential tools in a number of aspects". For example, the pulse techniques were used in optimising the structure of inter-gate dielectrics. The defect energy profiles provided by the pulse technique revealed that the source of poor memory retention of HfAlO is the presence of shallow electron traps [R1.1-R1.3]. It also identifies the traps at deep energy levels as responsible for the memory endurance problem with Al_2O_3 [R1.1-R1.3]. Through a delicate combination of these two dielectric materials, the device performance was optimised.

In relation to the significance and reach of the impact, Dr Van Houdt stated [C1.4]:

> "The performance of the 20-nm generation, as a result of using the high-k IGD layer, was enhanced significantly compared with the previous generation: cell size reduced by 30%, performance improved by 30%, and bit-cost reduced by 30%. The pulse techniques developed by LJMU researchers made an important and essential contribution to this development, an exemplar in terms of the impact of university research on industry. The revenue of Flash memory industry reaches well over $20 billion in 2013 and therefore the impact is significant and on a global scale."

As a result of the success of the 20-nm technology, Intel/Micron's NAND Flash memory revenue alone reached $4.19 billion in 2012, and its global market share increased to 22% from 19.5% in the previous year [C1.7]. Dr. Pierre Farzan, On-site Manager of Micron Technology Inc., confirmed that "the research work performed by LJMU is providing very valuable characterization techniques to our Consortium and add substantial value to the Flash memory program and industry" [C1.5].

5. Sources to corroborate the impact

[C1.1] The first collaboration agreement between the University and IMEC on memory devices (document available at http://www.ljmu.ac.uk/ENG/ENG_Docs/C1.1_-_IMEC_Collab_-_Agreement_-_2009.pdf). Contact Identifier Number: 1.

[C1.2] The second collaboration agreement between the University and IMEC (available at http://www.ljmu.ac.uk/ENG/ENG_Docs/C1.2_-_Imec_-_Collab_-_Agreement_-_FLASH_2012.pdf). Contact Identifier Number: 1.

[C1.3] The third collaboration agreement between the University and IMEC (available at the http://www.ljmu.ac.uk/ENG/ENG_Docs/C1.3_-_IMEC_-_Collab_-_Agreement_-_RRAM_2012.pdf). Contact Identifier Number: 1.

[C1.4] The statement, available at http://www.ljmu.ac.uk/ENG/ENG_Docs/C1.4_-_IMEC_Jan_support_statement.pdf. Contact Identifier Number: 3.

[C1.5] The statement, available at http://www.ljmu.ac.uk/ENG/ENG_Docs/C1.5_-_Micron_Tech_support_Statement.pdf. Contact Identifier Number: 4.

[C1.6] Contact Identifier Number: 2.

[C1.7] http://www.eetimes.com/document.asp?doc_id=1280394